Customer No.: 31561 Docket No.: 13353-US-PA

Application No.: 10/709,823

In the Specification:

[0029] FIG. 4 is a schematic block diagram illustrating the internal configuration of an

I/O unit according to a preferred embodiment of the present invention. Referring to

FIG. 4, a logic control unit 411 generates and provides an internal control signal to a

checking circuit 413, a data output latch 415, and a data input latch 417 according to a

control signal which is generated by the nonreal-time data interface unit 210 and

transmitted via the control bus. In addition, the logic control unit 411 provides an

acknowledgement signal "ack", which is used to indicate the current state of the I/O

unit 220. When it is required to transmit the nonreal-time data through the I/O unit

220, the nonreal-time data is transmitted to a bi-directional bus 41 via the data bus

first, and then the data output latch 415 extracts the nonreal-time data from the

bi-directional bus 41, and determines when to output the nonreal-time data via the

data output bus according to the control of the control logic unit 411. Oppositely,

when it is required to transmit the real-time data via the I/O unit 220, the real-time

data is stored into the data input latch 417 via the data input bus first, and then it is

determined whether to transmit the real-time data to the bi-directional bus 41 or not

according to the control of the control logic unit 411.

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